Remarks/Arguments:

I. Status

The Office Action dated July 1, 2004 (the "Office Action") has been carefully reviewed. Claims 2, 8, 12-14, 18, 20 and 22-24 have been amended. New claims 25-28 have been added. Accordingly, claims 2-10, 12-18 and 20-28 are pending in this application. Reconsideration of this application, as amended, is respectfully requested.

II. The Informalities in the Claims Have Been Corrected.

The Examiner objected to claims 1, 13 and 14 for including "adaptable to". The Applicants note that contrary to the assertion in the Office Action, MPEP 2106 does not identify "adaptable to" as language that *may* be indefinite. In fact, none of the language cited in the Office Action appears in MPEP 2106. Nonetheless, the wording in the claims has been amended to remove all instances of "adaptable to". The claims, as amended, recite particular steps or particular structure. Thus, the claims, as amended, are not indefinite.

III. The Rejections under 35 U.S.C. § 112 Have Been Overcome.

The Examiner objected to claims 8 and 22 for lacking antecedent basis. The claims have been amended to clarify the antecedent basis of the logical memory devices. Therefore, the Applicants respectfully submit that the limitations in claims 8 and 22 have sufficient antecedent basis.

The Examiner did not identify any prior art that included the limitations of claims 8 and 22. Therefore, the Applicants respectfully submit that claims 8 and 22 are allowable over

the prior art. Moreover, claims 8 and 22 depend directly or by way of an intermediate claim from claims 2 and 20, respectively and claims 2 and 20 have been amended to include additional limitations. Therefore, claims 8 and 22 are further allowable over the prior art.

IV. The Rejections under 35 U.S.C. § 102(a) Have Been Overcome.

In the Office Action, claims 2-4, 9, 10-15 and 20-21 were rejected under 35 U.S.C. 102(a) as being anticipated by U.S. Patent No. 6,721,271 B1 of Beshai et al. (hereinafter "Beshai"). Claim 11 has been cancelled and the remaining claims have been amended to include limitations not disclosed by Beshai.

Discussion Regarding Patentability of Claim 2

1. Beshai Does Not Disclose Sequential Writing of a Packet.

The Examiner rejected claim 2 based upon the proposition that Beshai disclosed writing a first, second and third portion of a received data packet to a first, second and third logical memory device. (Office Action at page 3). Claim 2, as amended, includes limitations not disclosed by Beshai.

Specifically, as amended claim 2 recites that the writing of a first, second and third portion of a received data packet to a first, second and third of a plurality of logical memory devices is done sequentially. One embodiment of a sequential writing step is shown in the flow diagram of FIG. 7 of the present application. As discussed in the specification, the method of FIG. 7 is performed during a single memory write access from a port. In contrast, Beshai discloses that during an access interval, all packet segments that are transferred are transferred to a single accessed memory section 66. (Beshai at column 10, lines 56-58). To

the extent the packet segments are from different data packets, the packet segments are sequentially routed to different memory sections 68 of the accessed memory section 66. (Beshai at column 10, lines 62-65). Thus, while Beshai does disclose that packet segments from a single data packet may be written to different memory sections 68 on different core memories (see e.g. Id. at column 11, lines 35-38), any such transfer is not sequential. Rather, the transfer would be effected during a separate access interval.

Accordingly, Beshai does not disclose the sequential writing of received data packet portions to different logical memory devices as recited in claim 2 as amended. Anticipation under 35 U.S.C. § 102 is proper only if the prior art reference discloses each and every element of the claim. Since Beshai does not disclose each and every element of Applicants' amended claim 2, Beshai does not anticipate claim 2. Therefore, the Applicants respectfully submit that the rejection of claim 2 under 35 U.S.C. 102(a) has been overcome.

Discussion Regarding Patentability of Claims 3-4 and 9-10

Claims 3-4 and 9-10 depend directly or by way of an intermediate claim from claim 2 and include the limitation discussed above with respect to claim 2. As a result, claims 3-4 and 9-10 are allowable for the reasons set forth above with respect to claim 2. Moreover, each of these claims include additional novel and non-obvious limitations. Accordingly, the Applicants respectfully submit that claims 3-4 and 9-10 are further allowable over the cited art.

Discussion Regarding Patentability of Claim 12

1. Beshai Does Not Disclose Writing To Multiple Memories During A Single Write Access.

The Examiner rejected claim 12 based upon the proposition that Beshai disclosed a memory controller operable to write a first, second and third portion of a received data packet to a first, second and third logical memory device. (Office Action at pages 4-5). Claim 12, as amended, includes limitations not disclosed by Beshai.

Specifically, as amended claim 12 recites that the writing of a first, second and third portion of a received data packet to a first, second and third of a plurality of logical memory devices is done during a single memory write access. One embodiment of a sequential writing step is shown in the flow diagram of FIG. 7 of the present application. As discussed in the specification, the method of FIG. 7 is performed during a single memory write access from a port. In contrast, Beshai discloses that during a single access interval, all packet segments that are transferred are transferred to a single accessed memory section 66. (Beshai at column 10, lines 56-58). Transfer of a packet segment to a second memory core can only be accomplished during a second access interval. (Id. at column 11, lines 35-38).

Accordingly, Beshai does not disclose writing received data packet portions to different logical memory devices during a single memory write access as recited in claim 12 as amended. Anticipation under 35 U.S.C. § 102 is proper only if the prior art reference discloses each and every element of the claim. Since Beshai does not disclose each and every element of Applicants' amended claim 12, Beshai does not anticipate claim 12. Therefore, the Applicants respectfully submit that the rejection of claim 12 under 35 U.S.C. 102(a) has been overcome.

Discussion Regarding Patentability of Claims 13-15

Claims 13-15 depend directly from claim 12 and include the limitation discussed above with respect to claim 12. As a result, claims 13-15 are allowable for the reasons set forth above with respect to claim 12. Moreover, each of these claims include additional novel and non-obvious limitations. Accordingly, the Applicants respectfully submit that claims 13-15 are further allowable over the cited art.

Discussion Regarding Patentability of Claim 20

Claim 20 is an independent method claim. However, claim 20 includes a step that requires writing received data packet portions to different logical memory devices during a single memory write access. This limitation is similar to the limitation discussed above with respect to claim 12. As a result, the Applicants respectfully submit that claim 20 is allowable for the reasons set forth above with respect to claim 12.

Discussion Regarding Patentability of Claim 21

Claim 21 depends directly from claim 20 and includes the limitation discussed above with respect to claim 20. As a result, claim 21 is allowable for the reasons set forth above with respect to claim 20. Moreover, claim 21 includes additional novel and non-obvious limitations. Accordingly, the Applicants respectfully submit that claim 21 is further allowable over the cited art.

V. The Rejection of Claims 5-7 and 16-18 under 103(a) Has Been Overcome.

In the Office Action, claims 5-7 and 16-18 were rejected under 35 U.S.C. 103(a) as being obvious over Beshai. The claims depend from claims amended to include non-obvious limitations. Therefore, the rejection has been overcome.

Discussion Regarding Patentability of Claim 5

1. The Discussion of Claim 2 Applies to Claim 5

The Examiner infers that Beshai allegedly discloses most of the limitations of claim 5, and relies upon Official Notice for the limitation of a first and second memory controller with a shared address line. (Office Action at page 6). The proposed modification does not arrive at the claimed invention

Claim 5 depends by way of claims 3 and 4 from claim 2 and incorporates all of the limitations of claim 2. For the reasons set forth above with respect to claim 2, Beshai does not disclose the sequential writing of packet portions. Modification of Beshai to include a first and second memory controller with a shared address line does not arrive at sequential writing of packet portions.

Therefore, modification of Beshai as proposed in the Office Action does not arrive at the invention of claim 5 as amended. Accordingly, the Examiner has failed to present a *prima facie* case of obviousness and the rejection of claim 5 under 35 U.S.C. 103(a) has been overcome.

Discussion Regarding Patentability of Claims 6-7

Claims 6 and 7 were rejected upon the same basis as claim 2, with further Official Notice of the obviousness of the use of SDRAMs and/or SSRAMs. (Office Action at page 6). Claims 6 and 7 depend directly from claim 2 and include the sequential writing limitation discussed above with respect to claim 2. Accordingly, even if Beshai is modified to include SDRAMs and/or SSRAMs, such a modification does not disclose the sequential writing limitation of claim 2. Therefore, the proposed modification does not arrive at the invention of claims 6 and 7 and the Applicants respectfully submit that claims 6 and 7 are allowable over the cited art.

Discussion Regarding Patentability of Claim 16

1. The Discussion of Claim 12 Applies to Claim 16

The Examiner infers that Beshai allegedly discloses most of the limitations of claim 16, and relies upon Official Notice for the limitation of a first and second memory controller with a shared address line. (Office Action at page 6). The proposed modification does not arrive at the claimed invention

Claim 16 depends by way of claim 15 from claim 12 and incorporates all of the limitations of claim 12. For the reasons set forth above with respect to claim 12, Beshai does not disclose the writing of packet portions to different memory devices during a single memory write access. Modification of Beshai to include a first and second memory controller with a shared address line does not arrive at writing of packet portions to different memory devices during a single memory write access.

Therefore, modification of Beshai as proposed in the Office Action does not arrive at the invention of claim 16 as amended. Accordingly, the Examiner has failed to present a *prima facie* case of obviousness and the rejection of claim 16 under 35 U.S.C. 103(a) has been overcome.

Discussion Regarding Patentability of Claims 17 and 18

Claims 17 and 18 were rejected upon the same basis as claim 12, with further Official Notice of the obviousness of the use of SDRAMs and/or SSRAMs. (Office Action at page 6). Claims 17 and 18 depend directly from claim 12 and include the "single memory access" limitation discussed above with respect to claim 12. Accordingly, even if Beshai is modified to include SDRAMs and/or SSRAMs, such a modification does not disclose the "single memory access" limitation of claim 12. Therefore, the proposed modification does not arrive at the invention of claims 17 and 18 and the Applicants respectfully submit that claims 17 and 18 are allowable over the cited art.

VII. Claims 25-28.

Claims 25-28 have been added. These claims recite novel and non-obvious limitations. Accordingly, claims 25-28 are believed to be allowable over the prior art.

VII. Conclusion

Applicant respectfully requests entry of the amendments and favorable consideration of the application.

A prompt and favorable action on the merits is requested.

Respectfully Submitted,

MAGINOT, MOORE & BECK

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Harold C. Moore
Registration No. 37,892
Bank One Center/Tower
111 Monument Circle, Suite 3000
Indianapolis, Indiana 46204-5115